

an analyzing circuit portion including a predetermined semiconductor element on said semiconductor substrate in a region other than the region where said neutrons are detected, wherein no boron containing layer is provided on said analyzing circuit portion.

REMARKS

These amendments and remarks are being filed in response to the Office Action dated June 24, 2002. For the following reasons, this Application should be in condition for allowance and the case passed to issue.

No new matter is introduced by this amendment. The amendment to the specification corrects minor informalities. The amendment to claim 3 is supported by originally filed claims 1 and 2, and the specification at page 5, line 21 to page 6, line 27. The amendments to claims 4 and 5 are supported by originally filed claims 1, 2, and 3.

In response to the Examiner's request that the non-elected claims be canceled, Applicant restates the request that non-elected process claims 6-8 be rejoined and examined on the merits upon the allowance of the article claims, pursuant to MPEP § 821.04.

Claim Rejections Under 35 U.S.C. § 102

Claims 1 and 2 are rejected under 35 U.S.C. § 102(b) as being anticipated by Ross (U.S. Patent No. 3,227,876), Kitaguchi et al. (U.S. Patent No. 5,321,269) or Seidel et al. (U.S. Patent No. 5,940,460).

Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by Carron et al. (U.S. Patent No. 5,399,863).

These rejections are traversed, and reconsideration and withdrawal thereof respectfully requested. Claims 1 and 2 have been canceled. Therefore, these rejections are moot.

Claim Rejections Under 35 U.S.C. § 103

Claims 3 and 5 are rejected under 35 U.S.C. § 103(a) as being obvious predicated upon Ross in view of Hossain et al. (U.S. Patent No. 6,075,261), or Kitaguchi et al. in view of Hossain et al.

These rejections are traversed, and reconsideration and withdrawal thereof respectfully requested. The following is comparison of the invention as claimed and the cited prior art.

An aspect of the invention, per claim 3, is a semiconductor device for detecting neutrons comprising a semiconductor substrate and a boron containing layer containing isotope ^{10}B , the layer being formed on the semiconductor substrate. A PN junction is formed on a surface area of the semiconductor substrate below the boron containing layer. Electron - positive hole pairs are generated in a depletion layer of the PN junction by α rays generated by a reaction between the neutrons and the isotope ^{10}B . The neutrons are detected on the basis of the quantity of electric charge of the electron - positive hole pairs. An analyzing circuit portion including a predetermined semiconductor element to estimate an energy spectrum of the α rays is formed on the semiconductor substrate in a region other than in the region where the neutrons are detected.

An aspect of the invention, per claim 5, is a semiconductor device for detecting neutrons comprising a semiconductor substrate and a boron containing layer containing isotope ^{10}B , the layer being formed on the semiconductor substrate. A PN junction is formed on a surface area of the semiconductor substrate below the boron containing layer. Electron - positive hole pairs are generated in a depletion layer of the PN junction by α rays generated by a reaction between the

neutrons and the isotope ^{10}B . The neutrons are detected on the basis of the quantity of electric charge of the electron - positive hole pairs. An analyzing circuit portion including a predetermined semiconductor element is formed on the semiconductor substrate in a region other than in the region where the neutrons are detected, wherein no boron containing layer is provided on the analyzing circuit portion.

The Examiner does not point out where in the cited prior art a semiconductor device for detecting neutrons comprising an analyzing portion including a predetermined semiconductor element to estimate an energy spectrum of α rays formed on the semiconductor substrate in a region other than the region where the neutrons are detected, as required by claim 3, is taught.

The Examiner does not point out where in the cited prior art a semiconductor device for detecting neutrons comprising an analyzing portion including a predetermined semiconductor element formed on the semiconductor substrate in a region other than the region where the neutrons are detected, and wherein no boron containing layer is provided on the analyzing circuit portion, as required by claim 5, is taught.

The Examiner relies on Hossain to provide a teaching of an analyzing circuit and a detector on the same substrate. The analyzing circuit of Hossain includes a plurality of memory cells, and Hossain teaches that the boron containing layer "is disposed over each of the memory cells" (column 4, lines 55-56 and Figures 1B-1E, 2A-2C). The circuits disclosed by Hossain (FIG. 3) are memory arrays and decoders. Hossain does not disclose or suggest analyzing circuit portions that estimate an energy spectrum of the α rays, as required by claim 3. Further, the neutron detecting device of Hossain requires that the boron containing layer be disposed over a portion of the analyzing circuit. Hossain does not suggest that **no** boron containing layer is provided on the analyzing circuit portion, as required by claim 5.

The combination of Hossain, and Ross or Kitaguchi would not render the instant semiconductor device obvious. Kitaguchi does not cure the deficiencies of Ross and Hossain. One of ordinary skill in this art would not have been motivated to form an analyzing circuit portion on the semiconductor substrate that estimates an energy spectrum of the α rays, as required by claim 3. One of ordinary skill in this art considering the Hossain, Ross, and Kitaguchi references would be motivated to form the boron containing layer over a portion of the analyzing circuit, as taught by Hossain, rather than **no** boron containing layer on the analyzing circuit portion, as required by claim 5.

In rejecting a claim under 35 U.S.C. § 103, the Examiner is required to discharge the initial burden by, *inter alia*, making "**clear and particular**" factual findings as to a **specific understanding** or **specific technological principal** which would have **realistically** impelled one having ordinary skill in the art to modify an applied reference (neutron detecting semiconductor device) to arrive at the claimed inventions (neutron detecting semiconductor device analyzing circuit portions that estimate an energy spectrum of the α rays, or neutron detecting semiconductor device, in which the boron containing layer and analyzing circuit portion are formed on the semiconductor substrate but no boron containing layer is provided on the analyzing circuit portion) based upon facts, -- not generalizations. *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 57 USPQ2d 1161 (Fed. Cir. 2000); *Ecolochem Inc. v. Southern California Edison, Co.*, 227 F.3d 1361, 56 USPQ2d 1065 (Fed. Cir. 2000); *In re Kotzab*, 217 F.3d 1365, 55 USPQ2d 1313 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). That burden has not been discharged, as the Examiner has provided no factual basis for modifying the Ross, Kitaguchi, or Hossain neutron detecting devices to include a boron containing layer and analyzing circuit portions that estimate an energy spectrum of the α rays, as required by claim 3,

or to include a boron containing layer and an analyzing circuit portion on the semiconductor substrate, wherein no boron containing layer is provided on the analyzing circuit portion, as required by claim 5.

There is no factual basis in Ross, Kitaguchi, or Hossain to support the conclusion that one having ordinary skill in the art would have been led to form a neutron detecting semiconductor device with an analyzing circuit portion that estimates an energy spectrum of the α rays, or with a boron containing layer and an analyzing circuit portion on the semiconductor substrate, wherein no boron containing layer is provided on the analyzing circuit portion. The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.*, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1449 (Fed. Cir. 1997). The Examiner has not met the burden of identifying a source in the applied prior art for the required realistic motivation because neither Ross, Kitaguchi, or Hossain suggest an analyzing circuit portion that estimates an energy spectrum of the α rays, or a boron containing layer and an analyzing circuit portion on the semiconductor substrate, wherein no boron containing layer is provided on the analyzing circuit portion.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do

so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Kotzab, supra, In re Fine*, 835 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). There is no teaching, suggestion, or motivation to modify Ross, Kitaguchi, or Hossain to obtain the claimed neutron detecting semiconductor devices.

The only teachings of the claimed neutron detecting semiconductor device with analyzing circuit portions that estimate an energy spectrum of the α rays, and/or a boron containing layer and an analyzing circuit portion on the semiconductor substrate, wherein no boron containing layer is provided on the analyzing circuit portion is found in Applicant's disclosure. However, the teaching or suggestion to make a claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner's conclusion of obviousness is not supported by any factual evidence. The motivation for modifying the prior art must come from the prior art and must be based on facts.

Allowable Subject Matter

Claim 4 is objected to as being dependent upon rejected claims but would be allowable if put in independent form including all limitations of claims 1-4.

Applicant gratefully acknowledges the indication of allowable subject matter. Claim 4 has been amended to place it in independent form including all the limitations of claims 1-4. Applicant, therefore, submits that claim 4 is allowable.

In light of the above remarks, this application should be considered in condition for allowance and the case passed to issue. If there are any questions regarding these remarks or the

09/960,356

application in general, a telephone call to the undersigned would be appreciated to expedite prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000
Date: October 24, 2002
Facsimile: (202) 756-8087

McDERMOTT, WILL & EMERY

Bernard P. Codd

Bernard P. Codd

Registration No. 46,429



VERSION WITH MARKINGS TO SHOW CHANGES MADE**IN THE SPECIFICATION:**

The paragraph beginning at line 25 of page 4 has been amended as follows:

For the formation of the boron containing layer 4 there are known [a] several [method] methods. In one method, boron is simultaneously doped into a film formed by a CVD method. In another method, an interlayer insulating film is formed and then boron is doped by ion implantation. The degree of radiation-activity by [neutron] neutrons depends upon the number of isotopes ^{10}B existent in the boron containing layer 4. Accordingly, even if the concentration of the isotope ^{10}B in the boron containing layer 4 is low, it may be sufficient that the boron containing layer 4 is formed to be thicker. Inversely, when the concentration of the isotope ^{10}B in the boron containing layer 4 is high, the boron containing layer 4 can be made thin. Particularly, provided the concentration of the isotope ^{10}B in the boron containing layer 4 is set to fall within about $10^{20}/\text{cm}^3$ to $10^{23}/\text{cm}^3$, and more preferably provided the upper limit of the concentration is set to $10^{22}/\text{cm}^3$ or less, the neutron and ^{10}B are securely brought into reaction to effectively emit α rays.

IN THE CLAIMS:

Claims 1 and 2 have been canceled.

Claims 3-5 have been amended as follows:

3. (Amended) A semiconductor device [according to claim 2, further] for detecting neutrons comprising:
a semiconductor substrate;

a boron containing layer containing isotope ^{10}B , the layer being formed on said semiconductor substrate;

a PN junction formed on a surface area of said semiconductor substrate below said boron containing layer; wherein

electron - positive hole pairs are generated in a depletion layer of said PN junction by α rays generated by a reaction between said neutrons and said isotope ^{10}B , and the neutrons are detected on the basis of the quantity of electric charge of the electron - positive hole pairs; and

an analyzing circuit portion including a predetermined semiconductor element to estimate an energy spectrum of the α rays on said semiconductor substrate in a region other than the region where said [neutron is] neutrons are detected.

4. (Amended) A semiconductor device [according to claim 3] for detecting neutrons comprising:

a semiconductor substrate;

a boron containing layer containing isotope ^{10}B , the layer being formed on said semiconductor substrate;

a PN junction formed on a surface area of said semiconductor substrate below said boron containing layer; wherein

electron - positive hole pairs are generated in a depletion layer of said PN junction by α rays generated by a reaction between said neutrons and said isotope ^{10}B , and the neutrons are detected on the basis of the quantity of electric charge of the electron - positive hole pairs; and

an analyzing circuit portion including a predetermined semiconductor element on said semiconductor substrate in a region other than the region where said neutrons are detected, wherein the concentration of said isotope ^{10}B in said boron containing layer in said analyzing

circuit portion is lower than that of said isotope ^{10}B of said boron containing layer in the region where said [neutron is] neutrons are detected.

5. (Amended) A semiconductor device [according to claim 3] for detecting neutrons comprising:

a semiconductor substrate;

a boron containing layer containing isotope ^{10}B , the layer being formed on said semiconductor substrate;

a PN junction formed on a surface area of said semiconductor substrate below said boron containing layer; wherein

electron - positive hole pairs are generated in a depletion layer of said PN junction by α rays generated by a reaction between said neutrons and said isotope ^{10}B , and the neutrons are detected on the basis of the quantity of electric charge of the electron - positive hole pairs; and

an analyzing circuit portion including a predetermined semiconductor element on said semiconductor substrate in a region other than the region where said neutrons are detected, wherein no boron containing layer is provided on said analyzing circuit portion.